REMARKS

The Office Action dated July 31, 2006, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-10 and 16-23 have been allowed. Claims 11-15 are submitted for consideration.

Claims 11-15 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,754,216 (Wong). The rejection is traversed as being based on a reference that neither teaches nor suggests the novel combination of features clearly recited in independent claims 11-15.

Claim 11, upon which claims 12-15 depend, recites a method for communication of rate control messages between two switches. The method includes the steps of designating a first plurality of ports of a first switch by a first numbering scheme, and designating a second plurality of ports of a second switch by a second numbering scheme. The method also includes coupling a first link port of the first plurality of ports to a second link port of the second plurality of ports and configuring the first switch to generate a first rate control message at the first switch and relay the first rate control message to a first local communications channel of the first port. The method further includes configuring the first switch to perform a rate control function related to the second switch based on the first rate control message. The first plurality of ports and the second plurality of ports are configured to perform switching and rate control functions.

As outlined below, Applicant submits that the cited reference of Wong does not teach or suggest the elements of claims 11-15.

Wong teaches a switch fabric in communication with an Ethernet switch system. The switch fabric includes a switch processor, a memory and a FAD transceiver system for receiving and transmitting streams of cells over a high-speed data bus. The FAD transceiver includes a plurality of receive and transmit buffers, where there exists a set of buffers for every multiplex device with which the FAD is to communication. The FAD includes a logic unit, a receive buffer, a unicast transmit buffer and a multicast transmit buffer. The Ethernet switch system includes a plurality of multiplex devices that receive and transmit data packets from the FAD system and that are coupled to a plurality of Ethernet switches that route packets to external devices connected thereto. Col. 7, line 66-Col. 8 line 36 and Figure 3.

Wong further teaches that the switch processor communicates with the memory to obtain memory status information and to the logic unit of FAD. The switch processor controls signals to the logic unit for controlling the transmission and reception of packets and for storage and retrieval from the memory. Col. 8, lines 48-60. Figure 4 shows the switch fabric in communication with a plurality of external devices for receiving and transmitting data. As shown in figure 4, FAD include three groups of buffers, the first group being receive buffers, the second group being unicast transmit buffers and the third group being multicast transmit buffers. Col. 9, line 53-Col. 10, line 5.

Applicants submit that Wong simply does not teach or suggest each of the elements recited in claim 11. Claim 11, in part, recites designating a first plurality of ports of a first switch by a first numbering scheme, and designating a second plurality of ports of a second switch by a second numbering scheme, wherein the first plurality of

ports and the second plurality of ports are configured to perform switching and rate control functions. The Office Action alleges that the first plurality of ports of the present invention is equivalent to the FAD buffers that are part of switch fabric 300 of Wong. As presented in our previous Response, as is known to those skilled in the art, a port of a switch is an interface on a switch to which other devices can be connected. A buffer, on the other hand, is known to those skilled in the art as a temporary storage area. Thus, one skilled in the art would not equate the buffers of Wong with the first plurality of port of the present invention because they are different components that perform different functions.

Col. 12, lines 28-60 of Wong disclose that the multiplex devices of figure 4 are connected to the buffers of the FAD, on one end, and, on the other end, to port interface device chips (OctaPIDs), each of which include eight port interface device that are coupled to communicate with a plurality of different Ethernet switches. Therefore, Applicant submits that even the teachings of Wong show the difference in the functions of a port and a buffer. Applicant submits that, if as the Office Action alleges the switching fabric of Wong is equivalent to the first plurality of ports of the present invention, then there is simply no teaching or suggestion in Wong of designating a first plurality of ports of a first switch by a first numbering scheme, and designating a second plurality of ports of a second switch by a second numbering scheme, wherein the first plurality of ports and the second plurality of ports are configured to perform switching and rate control functions, as recited in claim 11.

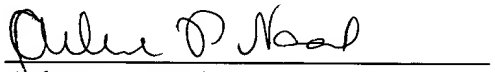
In the "Response to Arguments" section, the Office Action alleges that because "the FAD buffers of Wong are part of the switch fabric, these buffers are involved in the transmission and reception of data as well as control information between SWIP controller 414 and port interface device (OCTOPID) groups." Therefore, according to the Office Action, the buffers of Wong are configured to perform switching and rate control functions. As is known to one skilled in the art, switching functions include examining each packet entering a port and processing it accordingly rather than simply repeating the signal to all ports. As is also known to one skilled in the art, rate control functions include controlling inputs to the switch to avoid network congestion and packet dropping. While Wong discloses that each of FAD buffers 414-418 includes multiplexer that are used to select the specific buffer that is to transmit data SRAM memory or that is to receive data from the SRAM, there is simply no teaching or suggestion that the FAD buffers of Wong are configured to perform rate switching **and** control functions. Claim 11, in part, recites designating a first plurality of ports of a first switch by a first numbering scheme, wherein the first plurality of ports are configured to perform switching **and** rate control functions. Applicant submits that simply because a buffer is part of a switch does not mean that the buffer is automatically configured to perform switching **and** rate control functions. Furthermore, it would not be obvious to one skilled in the art, to configure a buffer to perform switching and rate control functions. Therefore, Applicants respectfully assert that the rejection under 35 U.S.C. §102(e) should be withdrawn because Wong fails to teach or suggest each feature of claim 11, and the dependent claims thereon.

As noted previously, claims 11-15 recite subject matter which is neither disclosed nor suggested in the prior art references cited in the Office Action. It is therefore respectfully requested that all of claims 11-15, in addition to claims 1-10 and 16-23, be allowed and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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